**CSU 5310 Computer Architecture Synopsis**

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| **Year** | 2 | | | | | |
| **Semester** | 1 | | | | | |
| **Course code** | CSU5310 | | | | | |
| **Course Name** | Computer Architecture | | | | | |
| **Credit value** | 3 | | | | | |
| **Core/Optional** | Core | | | | | |
| **Prerequisites** | 30 credits at Year 1 courses (Pass/Eligibility/Concurrent Registration) | | | | | |
| **Hourly breakdown** | **Theory** | | **Practical** | **Independent Learning** | **Assessments** | **Total hrs.** |
| 20 Sessions x 2  = **40 hrs.** | DS hrs. =  **14 hrs.** | Lab hrs. =  **18 hrs.** | Sessions (20 x 3) = **60 hrs**.  Online and other learning resources = 6 **hrs**.  Lab (12 x 0.5) = **10 hrs.**  Total **= 76 hrs.** | Continuous Assessments (CA) = **02 hrs.** | **150 hrs.** |
| **Course Aim/s.** | Introduce the science and art of selecting and interconnecting hardware components to create a computer that meets functional, performance and cost goals. | | | | | |
| **Programme Learning Outcomes (PLO)**  **addressed by course** | * **PLO1: Theoretical Knowledge:** Accumulate the fundamental knowledge in the area of Information Technology for analysing of problems, designing solutions. * **PLO2: Practical Knowledge and Application:** Make thorough judgments in accordance with basic theories and concepts and apply on Information Technology based solutions. * **PLO5: Creativity and Problem Solving:** Identify problems and develop solutions based on the information available using the concepts and theories. | | | | | |
| **Course Learning Outcomes (CLO)** | * **CLO1**: Understand the fundamentals of computer architecture (PLO1, PLO2) * **CLO2**: Articulate the design issues involved in computer architecture at theoretical and application levels (PLO1, PLO2) * **CLO3**: Design and implement single-cycle and pipelined datapaths for a given instruction set architecture (PLO1, PLO2, PLO5) * **CLO4**: Evaluate the close relation between instruction set architecture design, datapath design, and algorithm design (PLO1, PLO2, PLO5) * **CLO5**: Understand the performance trade-offs involved in designing the memory subsystem, including cache, main memory and virtual memory (PLO1, PLO2, PLO5) * **CLO6**: Evaluate analytically the performance of a hypothetical architecture (PLO1, PLO2,PLO5) | | | | | |
| **Content (Main topics, sub topics)** | 1. Introduction to the course and lab 2. Overview and history of computer architecture 3. Computer-aided design tools that process hardware and architectural representations 4. Hardware description languages – Verilog (Practical) 5. Basic organization of the von Neumann machine 6. Register Transfer Level (RTL) Design | | | | | |

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|  | 1. Finite State Machines (FSM) 2. Instruction set architecture 3. Programming abstractions, interfaces, use of libraries 4. Processor Design 5. Storage systems and their technology 6. Implementation of simple datapaths, including instruction pipelining 7. Hazard detection and resolution 8. Review of physical memory and memory management hardware 9. Input and output 10. Examples of I/O 11. Performance figures of merit Workloads and representative benchmarks, and methods of collecting and analyzing performance figures of merit | |
| **Teaching - Learning methods (TL)** | Self-Learning/Independent learning of Self-study   * Course material * Recommended reading * Online interactivity through MOODLE   Contact sessions   * Day schools, online classes non-compulsory * Laboratory practical exercises (compulsory) | |
| **Assessment strategy** | Overall CA Mark (OCAM): **40%** OCAM | Final Assessment: **60%** |
| Details:  Continuous Assessment (OCAM) Continuous Assessment (CA) CA I: **01 hr**. Continuous Assessment (CA) CA II: **01 hr**.  OCAM Computation  **OCAM =60 % of best CA I/CA II + 40% of other CAI/ CA II** | Theory: 100 % - **02 hrs.** (MCQ & Structured Essay) |
|  | **Overall mark = Z**  Z = 0.4 X + 0.6 Y, If Y ≥ 40.  Z = 0.4 X + 0.6 Y, If 30 ≤ Y < 40, subject to a maximum of 40. Z = Y, If Y < 30.  Condition for Pass:  Z ≥ 40 | |
| **Recommended Readings** | 1. Patterson, D.A. and Hennessy, J.L. 2011. *Computer Organization and Design: The Hardware/Software Interface*. 4th ed. Morgan Kaufmann Publishers. 2. Brown, S.D. and Vranesic Z.G. 2008. *Fundamentals of Digital Logic with VHDL.* 3rd ed. McGraw-Hill   Education. | |